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1A Processor:

Technology and Physical Design

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The physical design of large electronic switching systems (ESSs) requires a comprehensive set of technologies and design tools. The technology used for the 1A Processor and several ESSs consists of silicon integrated circuits, thin-film hybrid circuits, discrete component packaging, and apparatus to interconnect, power, and communicate with these devices. The application tools consist of comprehensive design guidelines and computer aids for circuit, logic, thermal, and physical design. In addition, computer aids are provided for documentation and preparation of information for manufacturing and testing. This paper uses text and illustrations to describe the design details and achieved performance of each of the major elements of the technology.

I. INTRODUCTION

1A technology is a standard set of devices, apparatus, and design tools which are used not only to design the 1A Processor and No. 4 ESS system, but also new switching systems such as No. 3 ESS[1] and additions to present systems such as the remreed network for No. 1 ESS.[2] It has been made a broad and flexible technology applicable to an entire new generation of telephone switching equipment.

The hardware design requirements of these "new-generation" switching systems differ in many important ways from the switching hardware typified in the No. 1 ESS system.[3] The advent of silicon and hybrid integrated circuits in the mid-1960s provided an opportunity for dramatic miniaturization in hardware. The first-level package in these new switching systems is often a silicon integrated-circuit chip about 50 thousandths of an inch square. Such a chip often contains more circuit

components than a 4- by 7-inch plug-in package in previous systems. The influence of miniaturization is characterized at every level of packaging by the reduced size and increased density of required interconnections.

Interconnections are also affected by another continuing trend, that of upgrading the performance of new switching equipment. Increased machine speeds and faster pulse rise times are required to provide more throughput and improved service. As the speed increases, so does the sensitivity to noise and transmission losses. As a consequence, stringent electrical requirements are imposed on the interconnections in faster machines such as the 1A Processor. Careful attention must be paid to the design of the interconnection system to insure that it meets all requirements.

An additional factor of importance in interconnections is cost. The conventional design, assembly, and wiring techniques used in previous switching systems have a relatively high labor content per interconnection. Rising labor costs and the need for more numerous and better controlled interconnections have been strong driving forces in the development of a hardware system with low labor sensitivity.

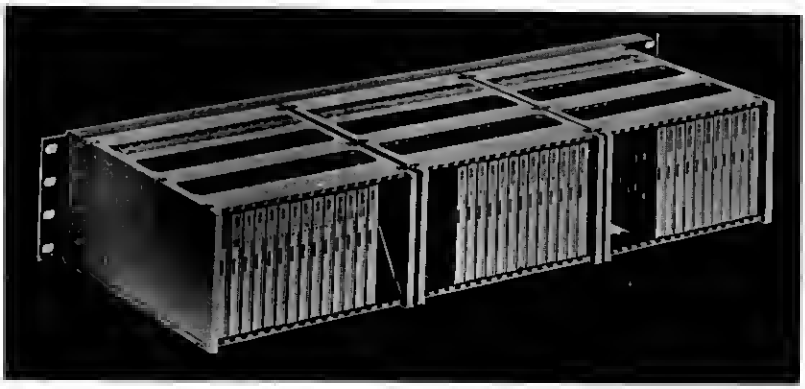
Three factors shaped the overall philosophy of 1A technology: miniaturization, high-speed electrical performance, and the need for low-cost design of manufacturing and assembly. Figure 1 contrasts 1A technology hardware with that used as building blocks for the No. 1 ESS system.

II. INTEGRATED CIRCUITS AND APPARATUS

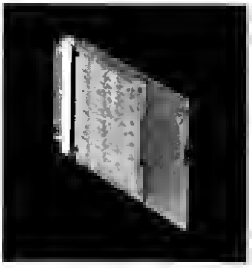
2.1 CDI-TTL integrated circuits

The design of the high-speed silicon integrated logic circuits evolved concurrently with the processor design in such a way that the overall system design was optimized. Choices of silicon integrated circuit (SIC) structure, processing, and logic gate design were based on general system performance requirements, available integration level, and the evolving physical design of the system during the 1968–1970 time frame.

Because of the processor cycle time, high-speed logic gates with propagation delays of from 5 to 10 ns were required. However, since relatively high gate packing density was desirable, and local frame ambient temperatures can reach 80°C (convectional cooling only), the gate power level had to he low. Accordingly, a low power-delay product was necessary. The combination of the collector-diffusion-isolation (CDI) structure[4–6] and the diode-modified transistor-transistor logic (DTTL) gate configuration provides a nominal power delay product better than 30 picojoules (for fanout = 1). This power delay product exceeded the best available at the time of the design, and provided a high gate density at low cost.



(a)



(b)

Fig. 1—Eight-bit adder comparison. (a) No. 1 ESS. (b) 1A technology.

Other system requirements, such as noise immunity, power distribution, and reliability influenced the choice of logic gate configuration, which evolved into a specific CDI-DTTL structure. Performance, reliability, and cost considerations finally dictated the adoption of a family of thirteen SIC codes, each embodied as a beam-leaded chip[7] of standard dimensions, and fabricated with a sealed junction technology.[8]

The CDI structure and processing, the CDI-DTTL gate design, and the SIC chip codes are discussed in the following.

2.1.1 CDI structure

Three device structures were considered for the 1A logic gates. These were the standard junction-isolated, buried collector (SBC), the air-isolated monolithic,[9] and the CDI structure.

The CDI offered the best combination of speed, power, and noise immunity, and, in addition, provided superior packing density and the simplest processing.

The CDI and SBC isolated transistor structures are compared in Fig. 2. In the SBC structure, the base and collector junctions are diffused into an n-type epitaxial layer, and a separate p+ isolation diffusion is required. In contrast, the CDI structure utilizes a buried n+ layer as its collector and a thin p-type epitaxial layer for the base region. It obtains isolation with a deep n+ diffusion, which also provides deep collector contact.

These differences make possible a 3-to-1 reduction in the required area of an isolated transistor, and reduce the number of required masked diffusion steps from five to three. It should be noted that the structure introduces some differences in electrical device parameters, notably in collector base breakdown voltage, inverse current gain, and device capacitances related to the collector structure. The CDI-DTTL circuit used in the 1A Processor chips maximizes the attainable performance for the CDI structure.

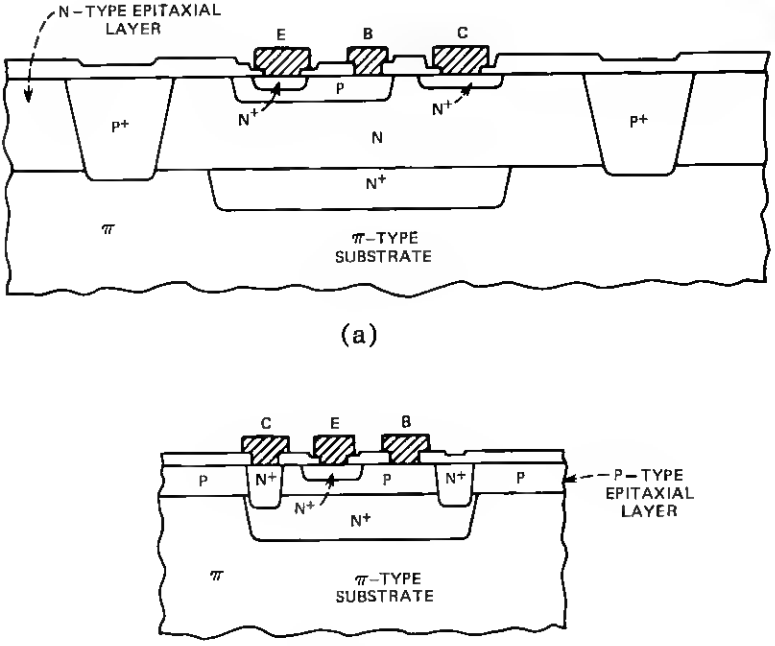


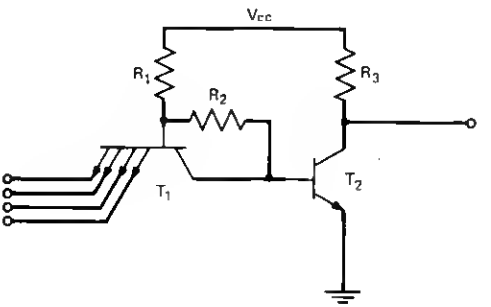
Fig. 2—Cross section of two transistor structures. (a) Standard, junction-isolated, buried collector (SBC). (b) Collector-diffusion-isolation structure (CDI).

2.1.2 CDI-DTTL gate configuration

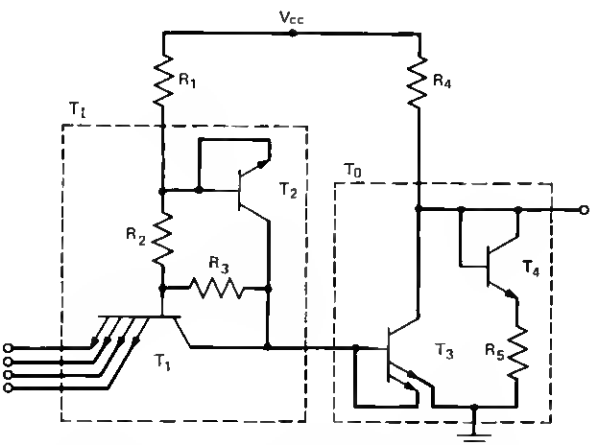
The objectives for gate performance included low-power, high-speed operation and ample noise margin for the operational junction temperatures of 0° to 90°C.

The basic gate shown in Fig. 3a can provide a power-delay product considerably better than other circuits, such as conventional TTL or ECL, primarily because it can be operated with reduced signal swings and low power-supply voltage. This circuit also allows outputs to be tied together to produce the wired AND function.

Taking this as a starting point, the gate design was modified to minimize the effects of higher inverse gain (α_I) and base collector capacitance



(a)



(b)

Fig. 3—(a) Basic TTL gate. (b) DTTL gate configuration for CDI.

associated with the CDI structure. As indicated in Fig. 3b, an input voltage divider network was added to the input circuit with a reference voltage obtained from a collector base diode. This serves to reduce and stabilize the effective α_I of the input array, and slightly increases the gate threshold. In addition, the output configuration has been modified by adding a diode clamp (T_4 and R_5) which controls the logic-1 level and reduces the gate propagation delay. Charge storage delays are minimized by the Buie clamp (emitter connected to base) on the output transistor, which acts to limit the degree of saturation.

The input and output structures shown inside the dotted lines in Fig. 3b (T_I and T_O) are readily fabricated as composite structures, resulting in an efficient layout with a minimum gate area.

This gate design provided performance consistent with system requirements for a power supply voltage $V_{CC} = 3.0 \pm 0.1$ V as follows:

(*i*) Propagation delay less than 5 ns for fanout = 1, nominal less than 7 ns for fanout = 3, and 20-pF loading.
(*ii*) Maximum fanout = 8.
(*iii*) Better than 200-mV minimum dc noise margins; temperature range 0° to 90°C.
(*iv*) Nominal power/gate = 6.3 mW.

2.1.3 Family of logic codes

A family of logic codes was developed to enable the synthesis of random logic functions with minimal design and assembly problems and a high degree of flexibility. The chips are all beam leaded to facilitate assembly on the thin-film hybrid circuits on which up to 52 chips can be interconnected. The chips are all identical in external dimensions (50 mils tip to tip), and each chip has 28 beam leads. The chips are protected during assembly and life with a junction seal[8] based on silicon nitride and, when utilized in conjunction with silicone rubber encapsulation, provide a highly reliable logic function.

The family of codes consists of six general-purpose codes and seven specific-function codes. General-purpose devices include a quad gate (two 3-input and two 5-input), a hex gate (four 2-input and two 3-input), a clipping hex, a clipping oct, a clipping input buffer (eight single RTL gates), and a dual high-power gate (two 4-input gates). The clipping gates are designed with special circuits to reduce ringing on long lines. The input buffer chip is designed to facilitate buffering between the backplane and the ceramic. The high-power gate, designed for driving high fanouts, low-impedance lines, large capacitances, or discrete devices, is designed with an active pull-up.

The seven functional chips are: a 2-bit register, a 2-bit register with gating, a gated delay flip-flop, a general-purpose translator, a dual-gated

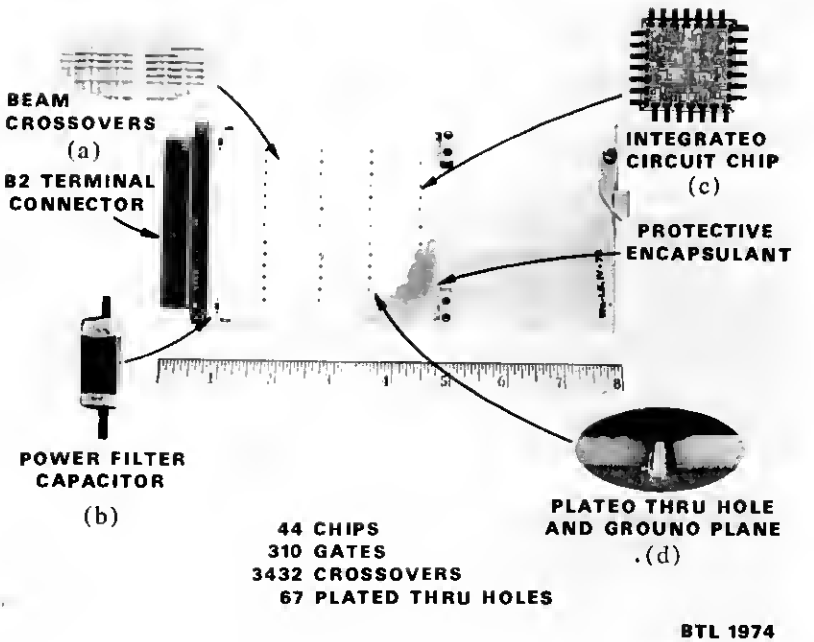


Fig. 4—Logic integrated-circuit packs.

quad, an unpowered dual-gated quad, and a dual-gated dual-gate configuration. The latter three codes are sets of gates with common gating leads.

The layout of these logic chips involved detailed attention to the effect of chip layout on ceramic wiring, since system packaging costs decrease with the number of gates per circuit pack, and increase with ceramic complexity. Underchip routing was also used advantageously where possible. Figure 4b is a microphotograph of a CDI-DTTL chip.

2.2 Hybrid integrated-circuit packages

Beam lead SICs of the types described in 2.1 are packaged and interconnected by the use of thin-film circuit patterns deposited on ceramic substrates.[10] These assemblies are termed HICs (hybrid integrated circuits). Two types of thin-film substrates are provided: a large 3.25- by 4.00-inch substrate which is the basis of a complete plug-in package and

a family of small substrates with dual-in-line or staggered leads interconnected on printed-wiring boards. The thin-film circuits are described in the following sections.

2.2.1 Thin-film circuits for FA circuit packs

Logic circuitry and other circuits, which can be built almost entirely of SIC chips and thin-film components, are packaged on 3.25- by 4.00-inch substrates of the type shown in Fig. 4. The chips are bonded to thin-film conductor patterns by a thermocompression bonding process[11] (Fig. 4c). There are predetermined locations for a maximum of 52 chips on the substrate. There are also 841 standardized locations for crossover arrays which provide a means for allowing conductor patterns to cross without making electrical contact (Fig. 4a). Each array consists of a matrix of crossovers[12] which allow a maximum of seven conductors to cross four bottom-level conductors. All crossovers on a substrate are fabricated simultaneously. Crossover counts on ceramics range from 250 to 4000.

The impedance of the thin-film conductors is controlled by choosing appropriate dimensions for the conductors and by providing a ground plane on the back surface of the ceramic, so that signal paths are 75-ohm microstrip transmission lines. Ground is distributed to each chip through laser-drilled, plated-through holes in the ceramic (Fig. 4d). Power is provided to each chip with a grid of wide, low-impedance, vertical and horizontal conductors. A pair of power filter capacitors are mounted on each ceramic circuit (Fig. 4b).

In some applications, thin films are used to provide resistors as well as interconnections. Circuit packs requiring resistors usually combine analog and logic functions on a single ceramic. As many as 50 SICs, 90 resistors, and 35 appliqued capacitors have been required on a single ceramic substrate.

As described in 2.4, a connector assembly is added to the thin-film circuits to form a complete plug-in circuit pack. The circuits are protected from corrosion, dust, and mechanical damage after assembly by a silicone rubber encapsulant.[13] The encapsulant can be removed for circuit repairs. A ceramic circuit pack is shown in Fig. 4.

Standardization of the design features of the ceramics and SICs permits the use of a comprehensive computer-aided design system (Section 3.4) and permits the manufacture of the 500 circuit codes required for ESS systems on a standardized manufacturing line.

2.2.2 Lead frame HICs

Circuitry which requires a combination of SICs and discrete components (power transistors, inductors, etc.) is not packaged on a large ce-

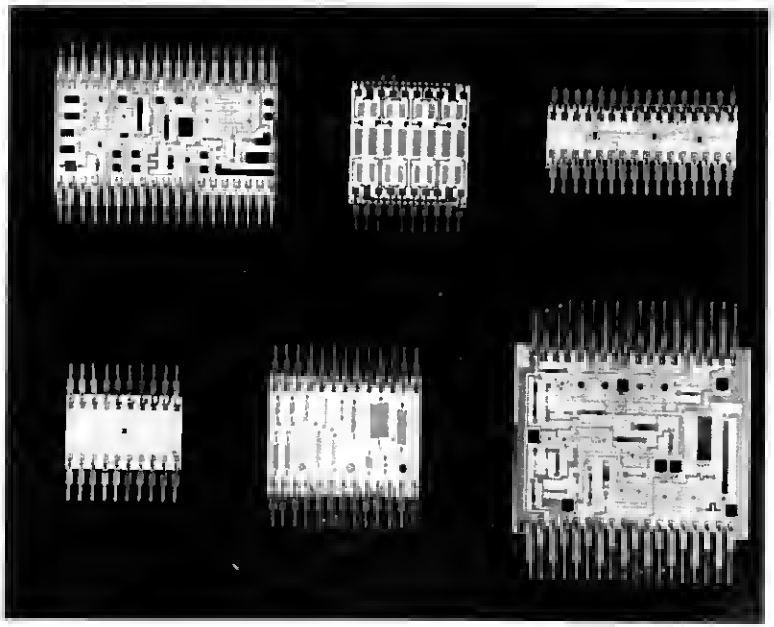


Fig. 5—Small hybrid integrated circuits.

ramic substrate. Instead, the SICs are bonded to thin-film circuits on small ceramic substrates. Dual-in-line or staggered leads are then thermocompression bonded to the substrate to form packages that can be inserted in printed-wiring boards for interconnection to other components. A representative sample of small HIC designs is shown in Fig. 5. Note that there are often many thin-film resistors and crossovers in addition to the thin-film interconnection patterns.

2.3 Discrete circuit packs

Circuits involving combinations of lead frame HICs and discrete components are packaged on discrete circuit packs.

The HICs are standoff mounted through holes on $\frac{1}{16}$-inch-thick epoxy-glass printed-wiring boards measuring 3.67 by 7 inches. A typical discrete circuit pack is shown in Fig. 6. Some of the packs require printed wiring on both sides of the board and in these cases plated-through holes are used to interconnect the two levels of wiring. However, many of the circuit packs use single-sided boards. All components and printed-wiring conductors are located on a standardized grid of 0.05 inch to facilitate computer-aided design and also to permit automated assembly and test.

Fig. 6—Discrete circuit.

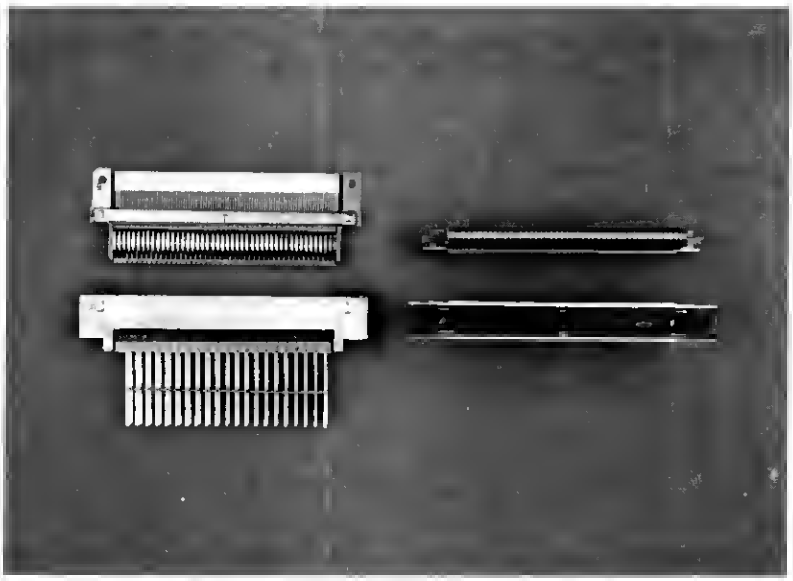


Fig. 7—Circuit-pack connectors.

An insulating cover coat is applied over all printed-wiring conductors to protect them from fingerprints and other contaminants that could degrade the insulation resistance of the pack. Conductors on the component side are coated before component assembly. The wiring side is coated after all assembly, mass soldering, and electrical testing is completed.

2.4 Circuit-pack connector

The circuit-pack connectors[14] shown in Fig. 7 link the circuit packs to the next higher level of assembly, the backplane unit. These connectors posed some difficult design problems because of the stringent requirements imposed by the physical and reliability needs of the system and also by the importance of low cost. Connector design requirements include a low and stable contact resistance over a 40-year life. This is particularly important in new systems, such as the 1A Processor, because of their low signal levels. Design requirements also include low contact surface wear for several hundred insertions and withdrawals, accommodation of manufacturing tolerances to permit low-cost manufacture, and a minimum end-of-life contact force of 100 grams. Further, a high contact density is required to be compatible with the high-density packaging needs of the 1A Processor. In addition, the high speed of the logic gates impose significant constraints on the electrical performance

of the connector. Controlled impedance is necessary as is a high degree of crosstalk isolation between contacts. Electrical performance of the connector is a key factor in establishing design concepts.

The plug half of the connector, which becomes a part of the circuit pack, contains the spring elements that apply the required contact forces. The individual contact springs have two distinct portions: a contact portion where electrical contact is made with a mating receptacle contact and a terminal portion where a permanent electrical connection is made with the circuit-pack conductor metallization. Deflection of the spring occurs in the area of the contact. The contact portion of the spring is beryllium copper and the terminal portion is either beryllium copper or copper, depending upon whether it is to be attached to a discrete pack by soldering or to a ceramic pack by thermocompression bonding.

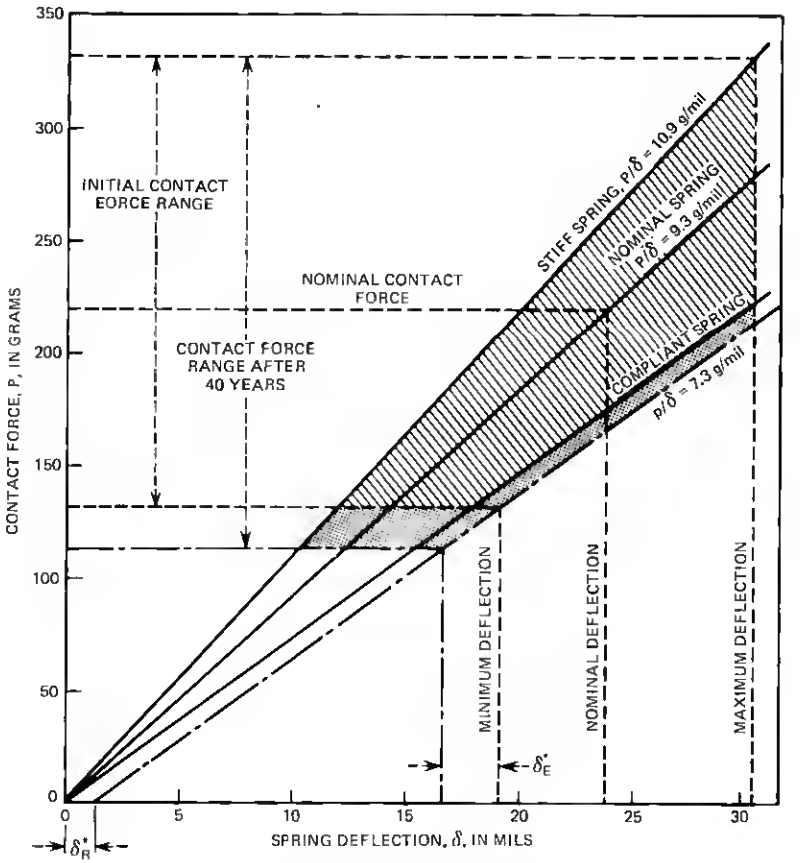
The contact portions of the springs are electroplated first with a nickel underplate and then with a wear-resistant gold alloy. The terminal portions are plated with 24K gold. Connectors are available with either 42 or 82 contacts. Eighty-two contact versions are used for both ceramic and discrete circuit packs. The 42-contact design is used only for discrete packs.

The receptacle half of the connector, which becomes a part of the backplane unit, includes the mating contacts incorporated into a housing that protects the contact surfaces from damage. The housing also locates the circuit-pack plug correctly so that upon insertion, the necessary mating contacts are in proper alignment. Metal side plates riveted to the housing serve two functions. They resist the load due to the contact force of an inserted plug connector and they provide a supplementary electrical ground to the frame.

The receptacle contacts do not deflect. They are made from a copper-nickel-tin alloy with a 24K gold strip inlaid in the contact area. The terminal ends of the contacts are formed so that the double row of contacts inside the housing is converted into four columns of terminals (in the case of the 82-pin connector) for backplane interconnections. The terminals are 0.025 inch square and are located on $\frac{1}{8}$-inch centers in both the horizontal and vertical directions. The 42-contact connector is similar, except that it has only two vertical columns of terminals and these are located on $\frac{1}{4}$-inch horizontal centers. Both the plug and the receptacle have special power and ground contacts to provide low resistance and low inductance. Dedicated power and ground terminals appear at each end of the connector, with two ground terminals in the center.

The contact force of the connector is affected by many factors, as is shown in the force deflection curve of Fig. 8. Variations in the spring properties of the beryllium copper material or its dimensions can, for a given deflection, appreciably affect the contact force. The extent of

this effect is indicated by the curves in Fig. 8 labeled "stiff spring" and "compliant spring." The contact force will also be affected by variations in many of the piece-part and assembly dimensions in both the plug and receptacle. Stress relaxation in metallic parts and creep in plastic parts are other factors that will affect contact force. When all possible variations are considered and their effects determined, the contact force is found to vary from its nominal value of 220 grams to a maximum of 335 grams and a minimum end-of-life value of 113 grams.



δ_R^* = CONNECTOR SPRING HEIGHT RELAXATION

δ_E^* = CONNECTOR HOUSING OPENING EXPANSION

Fig. 8—Replaceable terminal connector, contact force window.

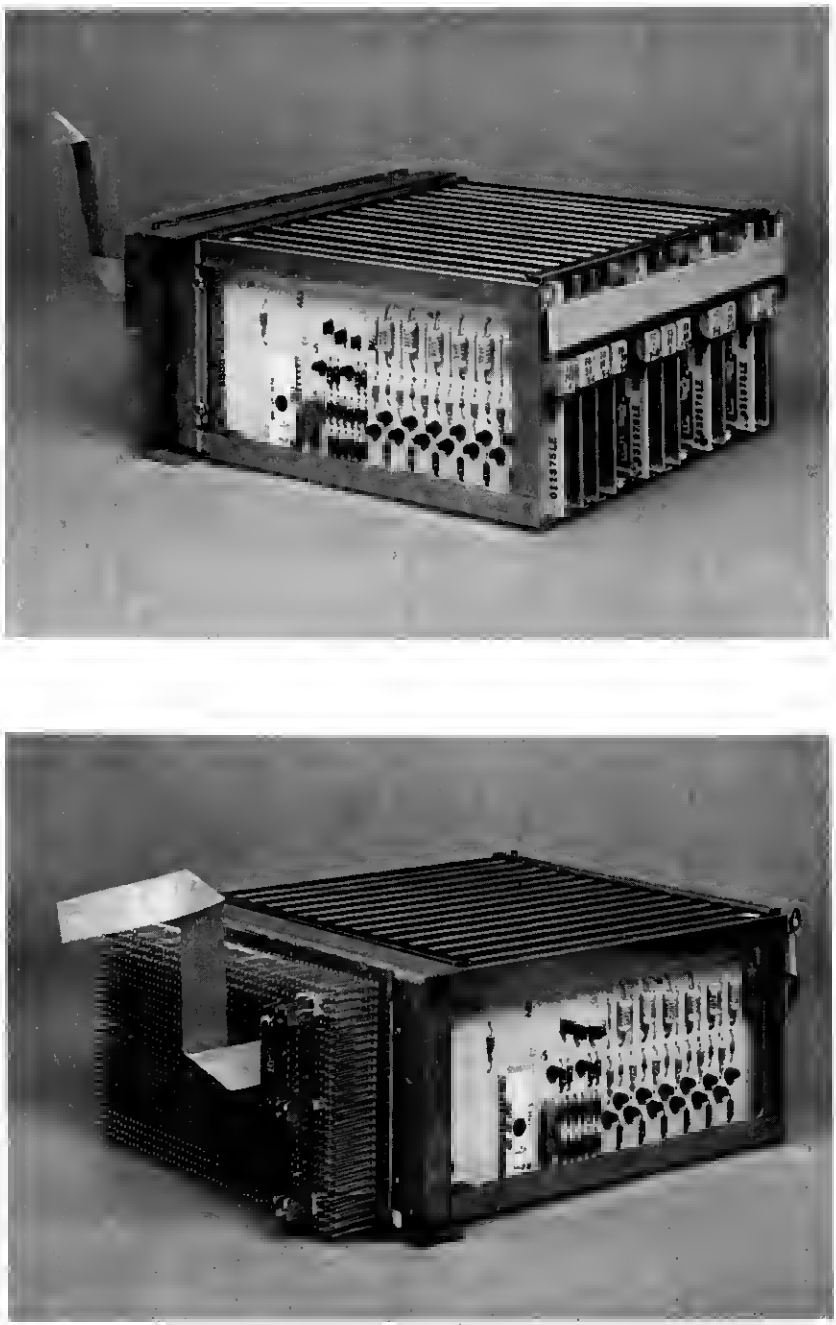


Fig. 9—Unit backplane.

2.5 Backplane unit

The next level of assembly is the backplane unit. This is built up of a number of circuit packs assembled on a common mounting structure and interconnected at the backplane to perform one or more specific functions. Generally, in a backplane unit the circuit packs are located on ½-inch horizontal centers (or multiples thereof) and 4-inch vertical centers. Occasionally, ¾-inch horizontal spacings are used.

The connector receptacles are secured to a mounting plate and apparatus mountings are added to the assembly, as shown in Fig. 9. The apparatus mountings serve to support the circuit packs and also provide alignment during insertion so that the circuit-pack plugs engage the receptacles correctly. The apparatus mounting is designed to provide a minimum impedance to the circulation of air past the circuit packs. A designation strip is provided on the front of the mounting so that the circuit packs can be readily identified. Package designations in the form of a letter-number combination are included both on the designation strip and on a plastic faceplate riveted to the front end of each circuit pack. Correct location of a circuit pack is assured by matching the code number of the circuit-pack faceplate with that in the apparatus mounting designation strip. Experience has demonstrated that this method provides adequate safeguards against incorrect pack insertions.

Interconnections between the circuit-pack receptacle terminals in a given backplane unit are accomplished by two methods. Multilayer boards are used for power and ground connections and some signal connections. Most of the signal connections, however, are made with 30-gauge wire that is machine wrapped. Electrically sensitive leads are applied manually, generally as tight-twisted pairs or miniature coaxial cables.

The multilayer boards range from 2 to 15 layers and vary in size from 4 by 8 inches to 12 by 22 inches. Interconnection between the various layers is accomplished with plated-through holes 0.040 inch in diameter after plating. The holes are located on ⅛-inch centers in both directions to match the terminal spacing of the circuit-pack connector.

Multilayer boards are assembled to the backplane unit, as shown in Fig. 9. Each terminal of the connector protrudes through a plated-through hole. A mass soldering operation completes the assembly of the backplane. In this process, each terminal is soldered to an external plated-through hole land on the multilayer board. The design of the board determines the connectivity between the connector terminal and the internal layers of the multilayer board.

Although the circuit-pack connectors are mounted on 4-inch vertical centers, their terminals occupy only 2½ inches of this dimension in the backplane terminal field. The balance of the area is filled with additional

terminals (0.025 inch square) used for terminating coaxial cables and tight-twisted pairs. In the 1A Processor, coaxial cables originate and terminate on these terminals rather than on the connector terminals. Machine-wrapped 30-gauge wires are used for the connections between the connector terminals and the coax terminating field. This practice restricts coax congestion to the areas between connectors where wire guides can be located and leaves the connector terminal field relatively unobstructed for trouble shooting and for accepting cable connectors.

The connector terminals and the coax terminating field terminals extend past the multilayer board for a length sufficient to accommodate two wire-wrapped connections. There is also enough additional length to permit cable connectors to be plugged directly onto the connector terminals. Special versions of connectors are available with gold plated terminal tips so that they can serve as male contacts for the cable connectors.

2.6 Frame

The final level of packaging is the frame that consists of one or more backplane units mounted on a common structural frame. Interconnection at this level may be between backplane units on the same frame or between different frames. In either case, it is accomplished witb connectorized cable assemblies. All 1A Processor backplane units are designed to be mounted from the front of the frame. These two features reduce frame assembly and test costs, and facilitate field maintenance and growth.

The contacts used in the cable connectors are of a box-type construction designed to mate with 0.025-inch-square male terminals. These contacts are incorporated into a molded plastic housing to form a connector assembly with contact spacings that are compatible with those of the circuit-pack connector terminals. There are 10- and 20-contact versions of the connector available. A 24K gold button is welded at the appropriate point in each contact to form its contact finish.

The design requirements for the cable connector are similar to those of the circuit-pack connector. Contact force of the cable connector varies from a nominal value of 260 grams to a maximum of 365 grams with a minimum end-of-life force of 112 grams.

For attachment to cables, the connector assemblies are mounted on small printed-wiring boards, as shown in Fig. 10. The cable wires are also terminated on the board, and printed conductors interconnect the cable wiring with the female contacts of the connector. The solder joints of the cable wires are stress relieved by the addition of small plastic clamps that are riveted to the board so that they clamp the cables securely.

Two basic types of cable are used for backplane unit or frame inter-

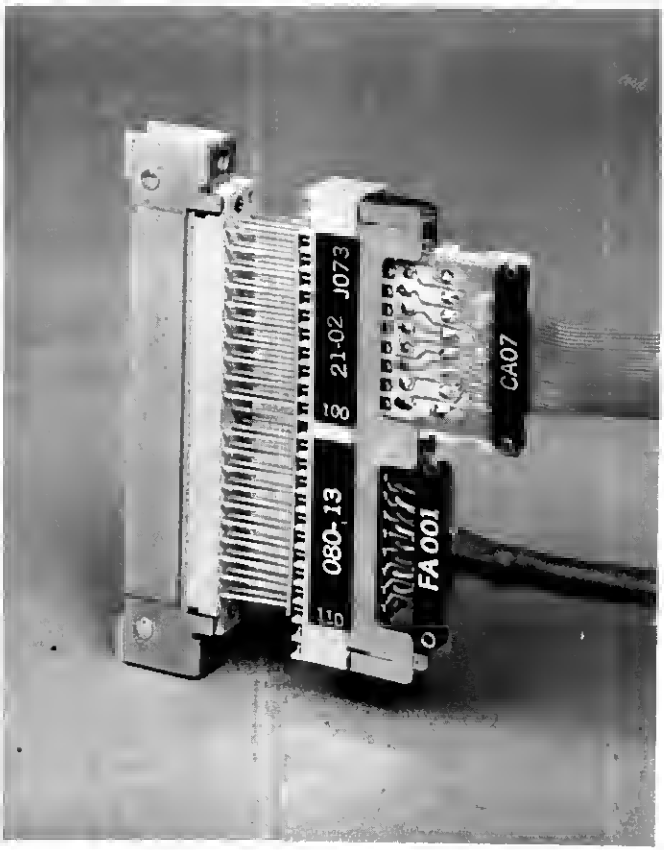


Fig. 10—Backplane cable connectorization.

connections. They are switchboard cable and flat tape cable. The switchboard cable is used for the transmission of balanced signals. It is composed of a number of pairs (usually eight) of tight twisted 26-gauge wire, with pvc insulation. The cable is contained inside a pvc jacket for abrasion resistance. The flat tape cable is used for dc or unbalanced signal transmission. A widely used version of flat tape cable contains 31 parallel conductors of 30-gauge wire spaced on 26-mm centers and imbedded in Teflon.* Only eight of the wires are used for signal transmission with the remaining 23 being used for grounds. Three ground wires are interposed between each signal wire for crosstalk isolation.

* Registered trademark of E.I. Dupont de Nemours & Co.

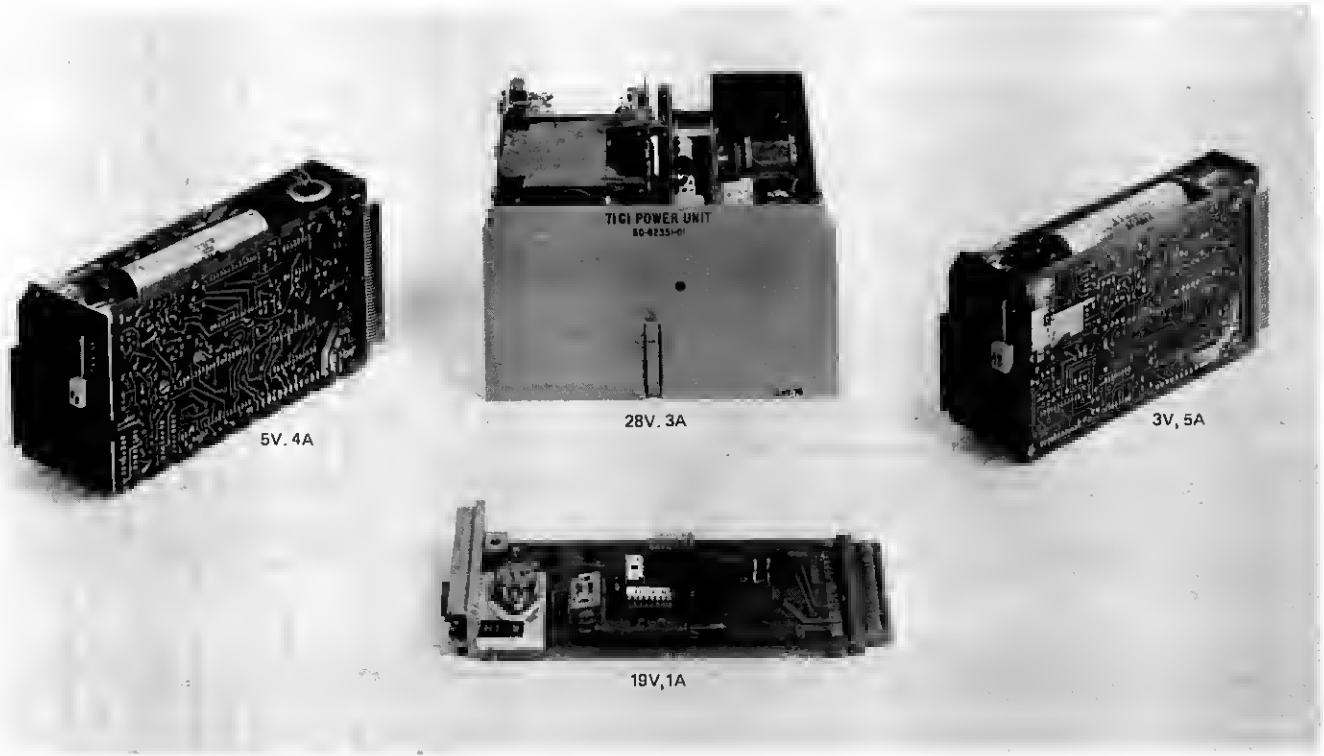


Fig. 11—1A technology power supplies.

2.7 Power supplies

The design of power supplies for the 1A Processor was based on commonality within the family, performance consistent with 1A technology, pluggability, extended environmental performance, and low cost. To achieve these characteristics the following criteria were met:

(*i*) Members of the family have a common physical format and incorporate standard codes of components and subassemblies.

(*ii*) The family of power supplies are mountable in standard apparatus housings and can be installed either adjacent to or remote from the circuitry it powers.

(*iii*) All power supplies are pluggable using standard 1A connectors and operate from −48 V and +24 V.

The result is a family of power modules (see Fig. 11) that have many common features, thereby enhancing overall manufacture. A detailed description of the power supply design is covered elsewhere.[15]

To complement the use of the power supply, a common use circuit pack was developed to be used in each frame. This pack is used to implement automatic power alarm testing, monitor power system status, and control the power switch. The power switch (see Fig. 12) developed for each independent power system (i.e., a frame or unit) is used for switching high currents, signaling, controlling status lights, fuse alarms, and lamp testing. The switch provides two pushbuttons on the front face for turning the power on or off. Visual power system status is provided by four lamps located on the front face. The switch, in conjunction with the power supply and common pack, provides a comprehensive means of providing power to the individual units.

III. TECHNOLOGY DESIGN AIDS

3.1 Crosstalk and noise margin design

All aspects of noise generation were extensively analyzed. These sources included connector crosstalk, stripline coupling on thin-film ceramics, backplane wiring coupling and EMI susceptibility, ground and power transients, resistive losses, etc. Each of these sources was correlated with physical design parameters and the total noise margin was allocated among the individual sources in a manner designed to minimize overall hardware costs. The approximate allocations used were 30 percent for the connector, 10 percent for ceramic-circuit-pack interconnection, 50 percent for backplanes, and 10 percent for all other sources.

The development intervals were minimized by using these allocations to develop a set of interconnection guidelines that provided audit thresholds for computer screening of potential trouble areas. This re-

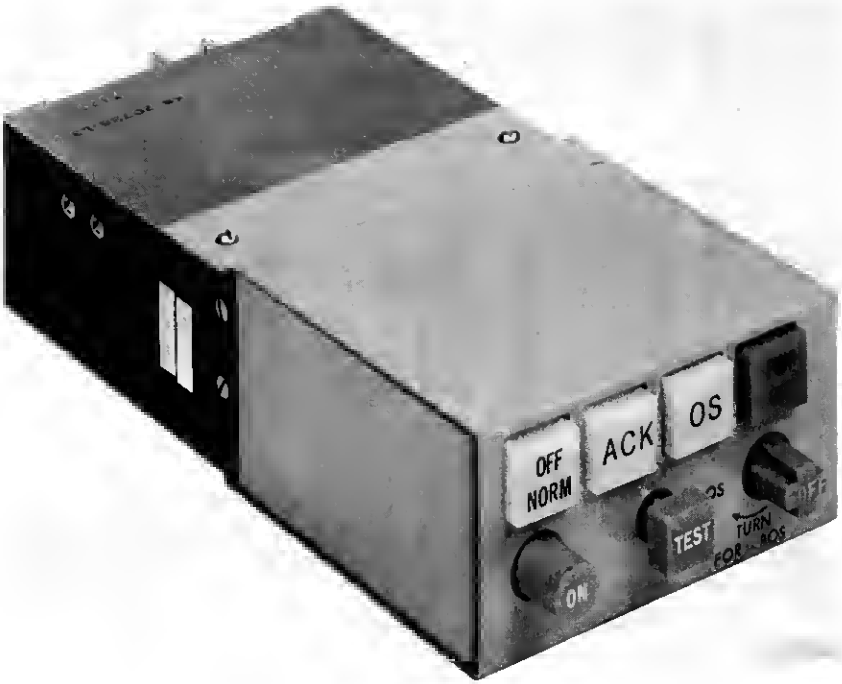


Fig. 12—Frame power and control switch.

lieved design engineers of much of the normal noise analysis and increased accuracy.

3.2 Timing analysis programs

To accurately predict critical timing delays in logic chains efficiently, two computer-aided design programs were developed in conjunction with the technology. The first program is an interactive program designed to implement the delay calculations outlined in a comprehensive electrical design guide developed for the technology. The delays through each gate are broken up into three components: intrinsic gate delay, delay due to capacitive loading, and signal propagation delay in the interconnections. In a typical path, these components may account for 50, 40, and 10 percent of the delay time, respectively. The parameters used in the program include worst-case gate characteristics, type and number of driven gates (loads), the number of load resistors, the number of collector tied outputs, the type and length of each wiring component, the type and number of connectors, the number of crossovers on the ceramic, the

Table I — Major thermal analysis programs

Topic	Program Name	Nature of Program
Silicon integrated circuits (SICs)	TASIC	Analytical
Ceramic and discrete circuit packs	FLAME	Analytical
Finned heat sinks	HEATSINK	Experimental
Frame thermal performance	FRAME	Experimental, analytical

length of adjacent wiring, and the type of the driven gate. These parameters can be entered manually or automatically from a design data base. Output is maximum, minimum, and typical propagation delay times.

For cases where the full analog characterization of the gates driving a transmission line interconnection media is necessary (typically long, high-speed, nets), the second program was developed. This program incorporates a lossless transmission line model and a library of gates modelled at the transistor level into an existing full-capability circuit-analysis program.

These programs have been used extensively in the design of ESS frames and typically predict delays to within 5 percent of actual measurements.

3.3 Thermal analysis programs

Thermal design aids were developed from both analytical and experimental studies to provide equipment designers with the tools to accurately predict device junction temperatures and optimize the use of natural convective cooling. These aids cover the whole range of design from SIC thermal analysis to entire frame thermal analysis. The major programs are shown in Table I. In addition to the specific design programs, extensive attention was directed towards the thermal optimization of 1A technology. Ceramic circuit-pack thermal performance was amplified through the incorporation of a metallic heat sink. Apparatus mountings and associated pack spacing were designed to maximize natural convection air currents while optimizing packaging density. Aids such as frame baffles and air channels were developed to further enhance thermal performance. As a result of this basic effort in apparatus design, the high-performance hardware, coupled with the previously mentioned programs, allowed the frame designers to densely pack the frame while assuring the required level of thermal performance.

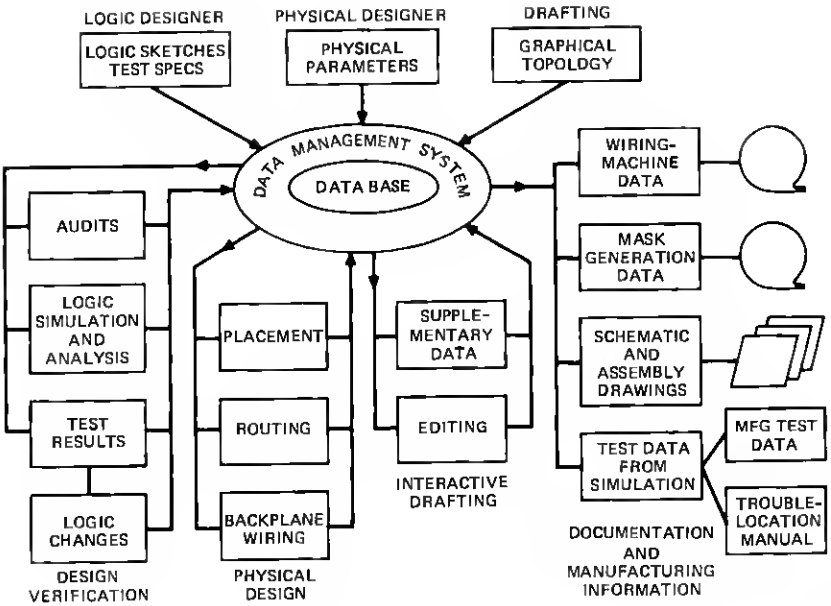


Fig. 13—Computer-aided development and manufacturing system.

3.4 Computer-aided development and manufacturing systems

A complete computer-aided development and manufacturing system was developed for 1A technology. It permits the design specifications to be introduced into a data base and enables their subsequent use by a variety of application programs (Fig. 13). Through these programs, the design is built and simulated in a general-purpose computer. The simulation allows the elimination of many clerical, encoding, and logic errors before any hardware is constructed. This data base, in conjunction with application programs, is used to do the partitioning, layout, and routing of the ceramic circuit packs. Extensive audits, such as crosstalk exposure, loading, etc., are incorporated to ensure adequate electrical design margins. While most programs are automatic, the capability is also available for interactive design in preparing circuit designs and test programs. Interactive capability is also provided to add supplementary data and edit the design.

Manufacturing information is generated from this data base and is used by Western Electric to generate art masters for circuit packs and backplanes. This provides machine-readable information in controlling automatic wiring machines. To assure compatibility of test requirements with test facilities, Bell Laboratories and Western Electric jointly developed computer-controlled test facilities. This assured that the test

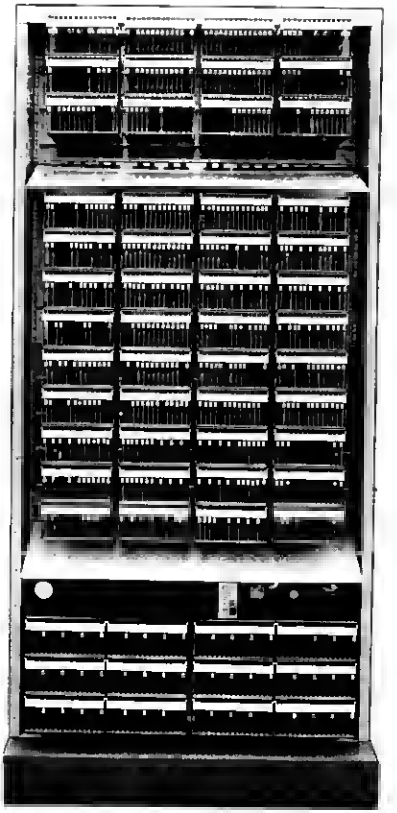


Fig. 14—Front view of central control.

information derived from the design data base could be used directly to test circuit packs, backplanes, frames, and systems during manufacture.

This same information is also used to generate documentation such as schematic diagrams and trouble location manuals furnished to the telephone companies. Figure 13 summarizes the features of the machine-aids system.

The machine aids have been invaluable for a development the size of No. 4 ESS. Without them it is questionable whether the job could have been done. Certainly it could not have been done on the schedule achieved.

IV. EXAMPLE OF 1A PROCESSOR FRAME

The central control frame provides a comprehensive example of a 1A Processor frame, as shown in Fig. 14. The circuit-pack equipment on each

CC frame is comprised of 234 logic packs, twenty-six 40-pin discrete circuit packs, two-hundred 80-pin discrete circuit packs, forty-eight 3-V power modules, and seven 19-V power modules. There are also a power control switch, fuse panels, and a number of general-purpose relays for power-control sequencing. This equipment is accommodated by a single-bay sheet-metal framework 7 feet high and 3 feet 3 inches wide. Structurally, this framework is identical to those used in No. 1 ESS except that the front-to-back depth is 1 foot 6 inches instead of 1 foot. The additional depth was utilized in the disk and core memory designs and also provided more wiring space for connectorization in the backplane.

Functionally, the CC circuit packs are subdivided as logic consisting of 50,000 gates on 250 ceramic and discrete circuit packs, communication bus consisting of 160 discrete packs, and power modules and associated fuses and control relays. As illustrated in Fig. 14, the first two levels are primarily equipped with communication-bus packs for the system peripheral units. The next seven levels accommodate the logic packs. The last three circuit-pack levels accommodate communication-bus packs for call stores, program stores, and auxiliary units. Power modules occupy the first three levels from the bottom of the frame, with fuses, power switch, and control relays being located directly above the power modules. The two horizontal gray panels are baffles that deflect heat from the power supplies to the rear of the frame. The design considerations for physical placement of these circuit packs were essentially (*i*) reliable circuit operation, (*ii*) manufacturing methods, (*iii*) installation methods, (*iv*) ease of maintenance, and (*v*) ability to implement changes. While these design considerations are not new, they were greatly influenced by measurable increases in device packing density, wiring terminals, switching speeds, and power dissipation per unit area. They were also influenced by the requirements for complete factory system tests.

Figure 15 shows the frame wiring consisting of 42,000 segments and associated hardware. Power and ground for the 3-V logic is implemented by means of multilayer printed-wire boards. This accounts for about 20,000 wire segments and provides for low-impedance power distribution to meet noise margin requirements of the high-speed logic devices. Of the remaining 22,000 wire segments, 90 percent are automatically wrapped, 30-gauge wires. The segment lengths for these wires are for the most part 13 inches or less. Longer segments are normally 75-ohm coax or 30-gauge twisted pairs, as determined by crosstalk susceptibility. A small number of wire segments are 100-ohm coax to provide for special clock pulse transmission. As indicated by Fig. 15, special wire guides are provided to retain the coax wiring in an orderly array and allow easy access to connector terminal field.

Interunit wiring logic connections between units are made by con-

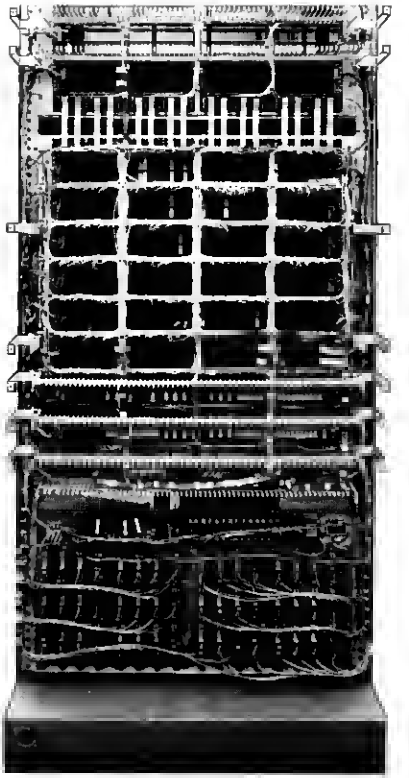


Fig. 15—Rear view of central control.

nectorized flat ribbon cables, as described in Section 2.6. The connectors are plugged either directly on wiring terminals or 80-pin connectors or on terminals of specially arranged connector fields. Interunit connections from the power unit to other units are also made by connectorized cable assemblies. These cables are made up of combinations of 14- or 16-gauge pairs, shielded 28-gauge pairs, and 26-gauge singles and pairs, as determined by power-interconnection requirements. This approach allows simplified unit replacement for repairs or design changes.

Interframe bus cable assemblies are connectorized lengths of 8-pair, 26-gauge sheathed cables. CC-to-CC logic interframe cable assemblies are connectorized flat ribbon cables. Power feeder cables from the power distributing frame are two pairs of 10-gauge wires for each CC. These cables are also connectorized and they are plugged into jacks located on the rear of the frame top channel.

As noted earlier, the frameworks for 1A Processor frames differ from those of No. 1 ESS only in that they are 1 foot 6 inches deep rather than

1 foot, and added depth is in the rear. In the case of the central control, the added depth is used to accommodate the volume of intraframe and interframe wiring and associated retaining hardware. With file stores and core stores, which account for most of the processor frames, added depth is used to accommodate the memory modules.

V. STANDARD FLOOR PLAN AND POWER SYSTEM

5.1 1A Processor floor plan

The 1A Processor utilizes a fixed floor plan with associated standard cabling and hardware (see Fig. 16). The fixed floor plan concept provides a number of significant advantages that assure the proper operation of the processor while minimizing overall cost. These advantages are:

(*i*) Line engineering is reduced to a minimum. Since there are no variations or options, decision making is almost nonexistent.

(*ii*) Manufacturing is simplified. All hardware, power and bus cable, cross-aisle racks, etc. are the same for all processors. All cables are pretested in the factory.

(*iii*) Installation interval is reduced to a minimum. Since every installation is the same and all cables are factory made, the processor can be installed in less than a week with a minimum of errors.

(*iv*) Growth of the processor is accomplished in an orderly fashion. Frames are grown only as sequentially numbered and always in the position indicated on the floor plan.

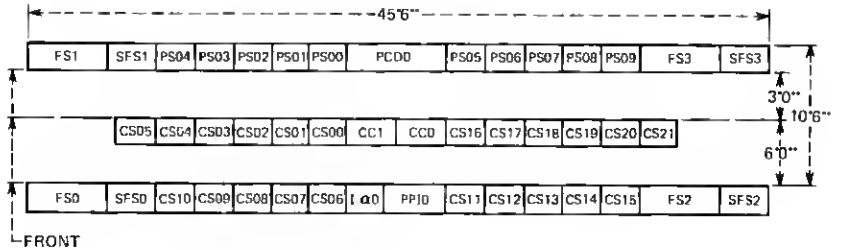
(*v*) Critical interframe bus timing is assured. Because of the critical timing parameters between the CC and the store frames, bus cable length is a critical factor. Since the cables are precisely made and tested at the factory, and not subject to installation circumstances, the pulse windows are guaranteed.

(*vi*) Thermal and floor-loading performance is optimized and assured. The fixed floor plan defines the boundaries of thermal flux and floor loading, thereby simplifying the office engineering.

While the fixed floor plan has sacrificed some installation flexibility, the advantages have far outweighed the disadvantages and have helped assure the high performance of the processor at overall minimum cost.

5.2 No. 1A Processor power system

Power in the 1A Processor has been integrated to a degree not found in earlier systems. From the −48 V energy source (battery or converter), power is supplied by duplicated feeders to the power conversion and



CC – CENTRAL CONTROL
CS – CALL STORE
PS – PROGRAM STORE
FS – FILE STORE
SFS – SUPLEMENTARY FILE STORE
PCD – POWER CONVERSION AND DISTRIBUTION
I/O – INPUT/OUTPUT
PPI – PROCESSOR PERIPHERAL INTERFACE

Fig. 16—Fixed floor plant of 1A Processor at full growth.

distribution frame (PCDF). This duplicated frame contains bulk −48 V to +24 V converters, +24 V and −48 V distribution filters, fuses, and built-in filter-charging facilities. A solid state fuse alarm and indicating system is employed that is testable under manual or system control. Newly developed, fast-blowing fuses are employed to minimize voltage transients caused by feeder faults.

Frames that are duplicated are fed power from one section of the PCDF. Nonduplicated frames are fed from both sections of the PCDF and the power is ORed at the frame. The dc-to-dc converters on the frame provide the required voltages and contain overcurrent detectors for fault detection and voltage monitors to assure in-range voltages. Standardized man-machine and frame-system interfaces are a feature of the power system and permit tests of the monitors and alarms. Particular attention has been paid to assure a reliable, safe, easily maintainable, and recoverable system.

VI. TECHNOLOGY PERFORMANCE

6.1 Electrical performance

One of the major challenges of the 1A Processor technology was to build complex, high-performance systems, such as No. 4 ESS, utilizing millions of logic gates with small signal swings, low noise margins, and low-power-supply voltages and, at the same time, to achieve a minimum of noise problems, high-speed operation at low power, and superior electromagnetic susceptibility and radiation performance. A number of factors permitted the use of low voltages including the low saturation

Table II — Failure rates (in FITs) of No. 4 ESS components and circuit packs in system labs

	Component Hr	Cumulative	Instantaneous	Objective
Ceramic circuit packs	2.8×10^8	733	310	450
CDI TTL integrated circuits	8.0×10^9	9	4	10
Connectors	6.2×10^8	9	$\ll 1$	19
Backplanes	7.5×10^{10}*	0.04	$\ll 1$	0.03
Power supplies†	1.9×10^7	1090	1700	2500

* Plated-through holes.
† Excludes three codes that are undergoing redesign.

voltage of the CDI process, the gate circuit design, careful design of the ground and power distribution, high-density packaging, controlled impedance wiring, and a comprehensive set of wiring rules, audits, product specifications, and controls. The net result was a fully characterized logic family and interconnection technology capable of achieving typical propagation delays of 7 to 10 ns (in a frame that includes all loading factors) at a power of 6 mW/gate. The controlled interconnections, high-density packaging, and power and ground distribution resulted in an electromagnetic susceptibility and radiation performance exceeding previous ESS systems, which used slower and higher noise margin logic families.

6.2 Reliability performance

The measured failure rates of 1A technology hardware are very low. A large amount of hardware has been built and placed in operation in the No. 4 ESS Systems Labs at Bell Laboratories in Naperville, Illinois. This equipment, plus that in the first commercial No. 4 ESS office in Chicago, provides a basis for measuring the reliability of the hardware. The unit of measure used to describe the failure rate of individual components is the FIT. One FIT is defined as one failure in 10^9 component operating hours. As can be seen in Table II, the cumulative failure rates are very near the objective failure rates established for long-term system operations. Much of the hardware upon which the reliability data of Table II are based is of early manufacturing vintage and has been exposed to much change activity. Nevertheless, the failure rates are approaching the objectives. The column labeled "instantaneous" in Table II represents the slope of the cumulative failure rate with time and can be regarded as representative of the current performance of the hardware. Note that the instantaneous failure rates are all below the objective failure rate. The reliability information obtained to date indicates that

the system will exceed its design objectives. The low failure rates of components indicate the success of a design philosophy that is based on careful and thorough engineering design using well tested and characterized materials and manufacturing processes. These create inherently reliable products and avoid "testing" or "burning in" reliability.

6.3 Thermal performance

Thermal considerations and design for the 1A Processor began very early in the development program. Strict attention was paid to maximizing the thermal performance of the hardware and developing techniques to analytically evaluate frame-temperature levels. As a consequence, even at the early prototype stage, thermal behavior of the frames was known under all limitations of design specifications and temperature environments (0° to 49°C office). As designs evolved and frames became available, thermal evaluation shifted from analytical to actual experimental testing under all environmental conditions. All frames were heat tested at elevated temperature and, when necessary, design improvements were implemented to assure proper functional performance. In all known cases, the operating device temperatures are consistent with noise margin, speed, and reliability requirements. Finally, the entire 1A Processor was heat tested as a system at the first No. 4 ESS installation. The system operated satisfactorily at the elevated temperature and the test proved to be effective in isolating a few remaining manufacturing and design problems.

6.4 Design intervals

The successful development of 1A Processor frames was highly dependent on the ability to rapidly proceed from a circuit schematic to the actual physical hardware. This feat was accomplished by the extensive employment of computer design aids, and the standardization of physical design topology. Since the basic frame apparatus, such as connectors, circuit-pack housings, mounting brackets, multilayer board backplanes, etc., were common among all frames, the availability was immediate and not dependent upon a design peculiar to that frame. Critical design intervals were limited to ceramic and printed epoxy circuit packs, along with the backplane-wiring interconnection system. Initially, digital, thin-film ceramic pack turnaround from circuit to complete pack was 13 weeks. However, as the technology matured the interval was reduced to four weeks. Comparable intervals for printed-circuit packs were 12 weeks and 5 weeks, respectively. Intervals for generation of backplane wiring information and actual execution were a function of number of wires and wire complexity, but usually were limited to five weeks. While these intervals reflect new designs, changes to existing circuits were

accomplished in much shorter time intervals when old hardware could be salvaged. As a result of these intervals, the development process was able to proceed in a manner consistent with program needs.

VII. ACKNOWLEDGMENTS

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